

ABSTRACT

A system and method for hardening an asynchronous combinational logic circuit against Single Event Upset (SEU) is presented. The asynchronous combinational logic circuit is located between two asynchronous registers. A fault detector is used to detect a fault at an output of the asynchronous combinational logic circuit caused by SEU. If the fault detector detects a fault, a first asynchronous register is prevented from clearing stored data and a second asynchronous register is prevented from loading data from the asynchronous combinational logic circuit until the fault is cleared. Further, a timer circuit is used to ensure enough time elapses to allow the asynchronous combinational logic circuit to reevaluate itself. The asynchronous combinational logic circuit reevaluates itself by first propagating a NULL wave front to clear the fault and then propagating the data stored in the first asynchronous register to its outputs.